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10/730,619	12/08/2003	Burkhard Becker	L&L-I0225	4277

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EXAMINER	
CHOE, YONG J	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,619	BECKER, BURKHARD	
	Examiner	Art Unit	
	YONG CHOE	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *1-3,5-8,11-15 and 18-23* is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *9,10,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The examiner acknowledges the applicant's submission of the amendment filed on 12/31/2007. At this point, claims 1,3,7,8,11 and 13 have been amended and claims 21,22 and 23 have been added. Claim 4 has been canceled to facilitate prosecution of the instant application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-3,5,6,11-15,18 and 20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hess (US Patent No.: US 4,405,980)** in view of **Tipon et al. (US Patent No.: 5,150,471)**.

Regarding independent claims 1 and 11, Hess discloses a method for transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit, the method which comprises:

associating the hardware arithmetic-logic unit (Fig.1: ALU) with at least one table memory (Fig.1 AKU), the hardware arithmetic-logic unit (Fig.1: ALU) obtaining data required during a computing operation (Fig.1: instruction) from the table memory (Fig.1:

AKU) and/or the hardware arithmetic-logic unit storing data computed during a computing operation in the table memory (col.5, lines 54~66); and

Hess further teaches providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule (Fig.1: ALU: It is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute addresses).

Hess does not specifically teach reading and/or writing from the digital processor to the table memory by:

preselecting a base address in the table memory dependent on a data type of data to be transmitted; computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware by taking the preselected base address as a starting point resulting in a computed plurality of address; and accessing the table memory with the digital processor using the computed a plurality of addresses for consecutive read access operations and/or consecutive write access operations in the table memory.

However, Tipon et al. teaches reading and/or writing from the digital processor (Fig.1: processor 12) to the table memory by:

preselecting a base address in the table memory (Fig.1: base address register 18) dependent on a data type of data to be transmitted; computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware (Fig.1: ALU 24) by taking the preselected base address as a starting point resulting in a

computed plurality of address; and accessing the table memory with the digital processor (Fig.1: processor 12) using the computed a plurality of addresses for consecutive read access operations and/or consecutive write access operations in the table memory (col.3, lines 15~32 and col.6, lines 6~29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the base address as taught by Tipon et al. into transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess in order to increase processing speed (col.2, line 10). Therefore, it would have been obvious to combine the base address as taught by Tipon et al. with transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess to obtain the invention.

Regarding claim 2, Tipon et al. teaches storing a plurality of base addresses associated with a plurality of different data types in a base address register, the base address that was preselected being one of the plurality of base addresses; and performing the step of preselecting the base address by using the processor to set a selection bit associated with the base address (col.3, lines 20-26 and col.6, lines 6~17).

Regarding claims 3 and 22, Tipon et al. teaches prescribing the plurality of base addresses unalterably in hardware (see Fig.1: base address register 18 and col.4, lines 5-15: the base address register is hard-wired.), wherein the plurality of base addresses cannot be processed by the digital processor (col.3, lines 15-32: the base

addresses of Tipon is not processed by the digital processor all the time. Thus, the plurality of base addresses cannot be processed by the digital processor)

Regarding claim 5, Tipon et al. teaches programming the base address (Fig.1: base address register) with the digital processor (Fig.1: processor 12).

Regarding claim 6, Tipon et al. teaches the digital processor, programming at least one information item selected from a group consisting of information relating to a number of data items being written to or read from a plurality of memory subareas associated with the base address, information about a block size of data blocks, information about a decoding rate, and information about utilized convolution polynomials (col.3, lines 49~56).

Regarding claim 12, Tipon et al. teaches said base address memory device is an external base address register designed such that in order to select the base address, said processor sets a selection bit associated with the base address (see Fig.1).

Regarding claim 13, Hess teaches said base address memory device is a read only memory (col.7, lines 1~5).

Regarding claim 14, Hess et al. teaches wherein said base address memory device is a rewritable memory that can be programmed by the digital processor (col.5, lines 54~57: RAM is a rewritable memory that can be programmed by the digital processor.).

Regarding claim 15, Tipon et al. teaches a configuration memory; said table memory including memory subareas; and said configuration memory for storing

information selected from a group consisting of information relating to a number of data items being written to or read from a plurality of said memory subareas associated with the base address, information about a block size of data blocks, information about a decoding rate, and information about utilized convolution polynomials (col.3, lines 49~56).

Regarding claim 18, Tipon et al. teaches wherein said table memory has a prescribed memory word length (col.5, lines 65~67).

Regarding claim 20, Tipon et al. teaches said hardware arithmetic-logic unit includes an equalizer hardware arithmetic-logic unit and a decoder hardware arithmetic-logic unit; said processor includes a data transmission connection to said equalizer hardware arithmetic-logic unit; and said processor includes a data transmission connection to said decoder hardware arithmetic-logic unit (see Fig.1).

Regarding claims 21 and 23, Hess further teaches providing the arithmetic computation rule by providing a hardware counter that implements the incrementation rule or a decrementation rule (Fig.1: ALU: It is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute addresses).

4. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hess (US Patent No.: US 4,405,980)** in view of **Tipon et al. (US Patent No.: 5,150,471)** and in further view of **Stafford et al. (US Patent No.: US 3,833,888)**.

Regarding claim 7, Hess and Tipon et al. do not specifically teach providing a first data type of the plurality of data types as soft input values for channel decoding that are intended for a Viterbi decoder hardware arithmetic-logic unit; and with the digital processor, programming how many soft input values per unit time can be stored in a memory subarea associated with the first data type

However, Stafford et al. teaches providing a first data type of the plurality of data types as soft input values for channel decoding that are intended for a Viterbi decoder hardware arithmetic-logic unit; and with the digital processor, programming how many soft input values per unit time can be stored in a memory subarea associated with the first data type (see abstract) (The Viterbi decoder hardware arithmetic-logic unit is an intended use for channel decoding. Thus, examiner will not give a weight on the Viterbi decoder hardware arithmetic-logic unit for purpose of examination).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the digital processor as taught by Stafford et al. into transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. in order to provide an enhanced controlling unit in a data processing system (col.2, line 41~42). Therefore, it would have been obvious combine the digital processor as taught by Stafford et al. with transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. to obtain the invention.

5. **Claims 8 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hess (US Patent No.: US 4,405,980)** in view of **Tipon et al. (US Patent No.: 5,150,471)** and in further view of **Serizawa et al. (US Patent No.: US 5,311,523)**.

Regarding claim 19, Hess and Tipon et al. do not specifically teach said hardware arithmetic-logic unit is a Viterbi hardware arithmetic-logic unit.

However, Serizawa et al. teaches said hardware arithmetic-logic unit is a Viterbi hardware arithmetic-logic unit (Fig.5 is a block diagram showing the structure of the Viterbi algorithm arithmetic).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Viterbi hardware arithmetic-logic unit as taught by Serizawa et al. into transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. in order to obtain good error rate performance (col.3, line 3).

Therefore, it would have been obvious to combine Viterbi hardware arithmetic-logic unit as taught by Serizawa et al. with transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. to obtain the invention.

Regarding claim 8, Tipon et al. teaches providing a second data type as trace back values computed by a decoder hardware arithmetic-logic unit; and with the digital

processor, programming how many states the trace back values need to include (see Fig.1).

Serizawa et al. further teaches computing data by a Viterbi decoder (Fig.5 is a block diagram showing the structure of the Viterbi algorithm arithmetic)..

Allowable Subject Matter

6. Claims 9&10 and 16&17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten claims 9&10 and claims 16&17 in independent form including all of the limitations of the base claim 1 and 11 respectively and any intervening claims.

Response to Arguments

7. Applicant's arguments filed on 12/31/2007 have been fully considered but they are not persuasive.

1st Point of Argument

Regarding Applicant's remarks on page 12, the applicants argue that the prior art does not teach or suggest computing the plurality of addresses in the table memory as an incrementation rule or decrementation rule and calculating the addresses of the main memory.

In response to applicant's argument, it is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules

such as incrementation or decrementation rule in order to compute data, address, etc,. And data from the main memory is transferred into ALU and outputted from the ALU. Thus Hess teaches providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule and calculating the addresses of the main memory. While this is unlike applicant's disclosed claimed method, this reads on broad claimed language

Conclusion

8. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication should be directed to **Yong Choe** at telephone number **571-270-1053**. The examiner can normally be reached on M-F 8:00am to 5:00pm. If attempts to reach the examiner by telephone are unsuccessful,

the examiner's supervisor, **Sanjiv Shah** can be reached on **571-272-4098**. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-irect.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YC
Yong J. Choe
Examiner / Art Unit 2185

/Gary J Portka/
Primary Examiner, Art Unit 2188

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/730,619	BECKER, BURKHARD	
	Examiner	Art Unit	
	YONG CHOE	2185	